DB

a gate oxide formed on said semiconductor substrate from said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation;

a source region and a drain region formed in said layer of polycrystalline silicon; and

a gate electrode formed on said layer of insulating material.

Remarks

Claims 9-12 and 14 are pending the application. Claims 9-12 and 14 have been rejected.

Specification:

The specification has been objected to for not complying with 35 USC § 112, first paragraph. The Examiner states that the specification has not been written to enable of person skilled in the art to form a source and drain in a substrate where the substrate comprises silicon dioxide, quartz, or glass. Applicant pointed out in the previous response that the specification does state that the source and drain can be formed by conventional doping techniques. However, the Examiner asserts that the fact that conventional doping techniques are used does not provide for adding dopants to an insulating substrate to form conductive regions. The Examiner further states that conventional doping techniques used to form source and drain regions are performed on a semiconductor substrate, not on an insulating substrate.

Applicant would like to clarify for the Examiner that the source and drain are not formed in an insulting substrate. The Specification teaches a semiconductor 206 that is formed over a substrate 202 wherein the source and drain are formed on the semiconductor 206. More specifically, the Specification describes a precursor 10 that includes a semiconductor substrate 12. The substrate 12 can be formed from silicon, gallium arsenide indium phosphide, polycrystalline silicon, silicon dioxide, glass and quarts. It is further explained that glass, quartz and silicon dioxide are particularly useful if the precursor 10 is further processed into a thin film transistor, such as described in

connection with Fig. 5. See page 7, line 18- page 8, line 1. Fig. 5 shows a thin film transistor 200 that includes an insulating substrate 202. A layer 204 of semiconducting material 206 is formed on the surface of the substrate 202. A source region 208 and drain region 210 are formed on the layer 204 of semiconducting material 206. The insulating substrate 202 can be glass, quartz or silicon dioxide. See page 13, lines 2-16 and Fig. 5. Furthermore, it is stated that the source 56 and drain 58 are formed by any conventional conductive doping technique. See page 11, lines 24-25. In addition, page 10, lines 22-23, has been amended to provide clarity. Thus, the Specification clearly enables one of ordinary skill to form a source and drain on a semiconductor.

The Examiner also states that the specification also has not been written to enable a person of ordinary skill in the art to form a layer of polycrystalline silicon on silicon dioxide by thermal oxidation. The specification has been amended to delete thermal oxidation from the process list on page 8, line 12, page 9, line 21, page 13, line 21, and page 14, line 15.

In light of the above amendments and arguments, applicant believes the specification is in compliance with 35 USC § 112, first paragraph.

Rejections under 35 USC § 112

Claims 9-12 and 14 have been rejected under 35 USC § 112, second paragraph as being indefinite. The Examiner claims that the phrase "free of metal contaminants" is unclear because one cannot ascertain the meets and bounds of the limitation. Applicant respectfully traverses this rejection. The Specification defines the problem of metal contamination on page 1. More specifically, it is explained that a Kaufman ion source sputters metal from a grid and the metal becomes implanted in the target causing the target to become contaminated. See page 1, lines 17-23. In addition, the Specification explains that using PSII reduces metal contamination because it does not use a metal grid. See page 10, lines 9-13. Thus, in light of the specification, it is evident to one of ordinary skill in the art what is meant by "free of metal contaminants." Therefore, the phrase "free

of metal contaminants" recited in claims 9-12 and 14 is definite and in compliance with 35 USC § 112, second paragraph.

Claims 10 –12 have been further rejected under 35 USC § 112, second paragraph as being indefinite. The Examiner states that it is unclear whether the gate oxide is the same oxide as claimed in line 3 of claim 10 or whether a second oxide layer is claimed. Claims 10-12 have been amended to recite that the "gate oxide[s] is formed...from said silicon dioxide layer." Thus, claims 10-12 are now in compliance with 35 USC § 112, second paragraph.

Rejections under 35 USC §112, first paragraph

Claims 9-12 and 14 have been rejected under 35 USC §112, first paragraph. The Examiner asserts that the limitation "free of metal contaminants" is not enabled in the specification as to how many metal contaminants or what species of metal contaminants can be present. As explained above, the Specification defines the problem of metal contamination when using the Kaufman ion source as metal sputters from a grid and contaminates the target. See page 1, lines 17-23. In addition, the Specification explains that using PSII reduces metal contamination because it does not use a metal grid. See page 10, lines 9-13. Thus, claims 9-12 and 14 are in compliance with 35 USC § 112, first paragraph.

Rejections under 35 USC § 102(a)

Claim 9 has been rejected under 35 USC § 102(a) as being anticipated by "Applicant's admitted prior art." The Examiner stated that on page 1, lines 12-16 of the Specification, "Applicant's admitted prior art" discloses a layer of silicon dioxide having been doped with hydrogen ions. The Examiner claims that it is implicitly understood that the polysilicon is formed seeing that the "admitted prior art" discusses performing the hydrogen doping of the silicon dioxide so as to provide a thinner, smoother polysilicon film deposited on the silicon dioxide. The Examiner states that it is implicitly understood that the layer of silicon dioxide is free of metal contaminants.

The "admitted prior art" does not teach doping the silicon dioxide layer with hydrogen ions using PSII. Rather, at page 1, lines 12-16, the "admitted prior art" process teaches the use of a Kaufman ion source to implant hydrogen atoms. Using the Kaufman ion source results in metal contamination as explained on page 1, lines 19-21. Therefore, it is not implicitly understood that the silicon dioxide layer is free of metal contaminants as asserted by the Examiner. To the contrary, it would be understood that the layer was contaminated with metal.

Rejections under 35 USC § 103 (a)

Claims 10-12 have been rejected under 35 USC § 103 (a) as being unpatentable over Burns et al. in view of "applicant's admitted prior art." The Examiner states that Burns et al. teaches a field effect transistor in fig. 9.8. Burns et al. does not teach that the substrate has hydrogen ions implanted therein or is free of metal contaminants. To cure this deficiency, the Examiner states that "Applicant's admitted prior art" teaches implanting hydrogen ions into silicon dioxide glass layer to provide smooth topology polycrystalline film. Thus, the Examiner concludes that the invention as recited in claims 10-12 would have been obvious.

Claim 10 recites "said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation, wherein said layer of silicon dioxide is free of metal contaminants." As shown above, the "admitted prior art" does not teach or suggest doping the silicon dioxide layer with hydrogen ions using PSII and having no metal contaminants in the silicon dioxide layer. The "admitted prior art" (i.e., use of a Kaufman ion source) produces a metal contaminated layer. Burns does not cure this deficiency. Therefore, even if the teachings were combined, the claimed invention would not be taught or suggested as Burns does not even mention using PSII to implant hydrogen ions nor does Burns mention a metal free silicon dioxide layer. Therefore, claim 10 is patentable over the "admitted prior art" combined with Burns.

Claim 11 recites "said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation, wherein said layer of silicon dioxide is free of

metal contaminants." As shown above, these limitations are not taught or suggested by the cited prior art. Therefore, claim 11 is patentable over the "admitted prior art" combined with Burns.

Claim 12 recites "said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation, wherein said layer of silicon dioxide is free of metal contaminants." As shown above, these limitations are not taught or suggested by the cited prior art. Therefore, claim 12 is patentable over the "admitted prior art" combined with Burns.

Claim 14 has been rejected under 35 USC § 103 (a) as being unpatentable over Murata et al. in view of applicant's "admitted prior art." Murata et al. does not teach a substrate having hydrogen ions implanted therein or being free of metal contaminants. In order to cure this deficiency, the Examiner asserts that Applicant's "admitted prior art" teaches implanting hydrogen ions into silicon dioxide glass layer to provide smooth topology polycrystalline film. The Examiner then concludes that claim 14 would have been obvious in view of the cited prior art.

Claim 14 recites "said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation, wherein said layer of silicon dioxide is free of metal contaminants." As shown above, the "admitted prior art" does not teach or suggest doping the silicon dioxide layer with hydrogen ions using PSII, the resulting layer having no metal contaminants. Murata does not cure this deficiency. Therefore, even if the teachings were combined, the claimed invention would not be taught or suggested as Murata does not even mention using PSII to implant hydrogen ions nor does Murata mention a metal free silicon dioxide layer. Therefore, claim 14 is patentable over the "admitted prior art" combined with Burns.

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In CONCLUSION

Applicant respectfully submits that, in view of the above remarks, the application is now in condition for allowance. Early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,

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